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SPECIFICATION FOR THE AGS BPM DIGITAL MULTIPLEXER BOARDS

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.0 INTRODUCTION

The boards in this specification are part of the of the AGS Beam Position Monitor(BPM) system upgrade. It will be part of the system which converts the 216 fiber optic outputs from the digital V/F converters in buildings A10, E10, and H10 into TTL signals. These TTL signals are then transmitted to local counters. A digital multiplexer is also included in this design to provide the MCR with any combination of 8 of these signals.

This specification describes boards that accept up to 256 fiber optic cables for the purposes of converting them to TTL signals. These signals are then used as inputs to a 256 X 8 digital multiplexer and as inputs to drivers for remote transmission. Remote control of the mux is through an Ethernet connection to a VME Front End Computer(FEC).

The 256 fiber inputs will be processed by 16 Data Boards each handling 16 signals. Each board will have 16 fiber optic receivers, 16 TTL differential drivers, a 16 X 8 Altera multiplexer chip, and an Altera VME interface chip. A 17th board will have the 8 fiber optic drivers for remote transmission of the mux output. These will be 9U VME boards.

The incoming signal frequency will vary from 8 to 10 MHz. The pulse width should have a minimum duration of 35 nanosecs. The duty cycle should not be less then 35 %.

Each 16 X 8 mux will be directly controlled by a FEC through a common J1/P1 backplane. The 17 boards are interconnected through a dedicated 17 slot J2/P2 backplane. The FEC and the V108 board will reside in 4 6U slots with a common but separate J2/P2 backplane. Separation of these backplanes will minimize crosstalk between the FEC and the 8 - 10 MHz outputs of the mux.

The TTL signals will be transmitted via a 64 wire ribbon cable to a bulk headed connector mounted on a rear panel. This will utilize the J3 P3 connector on each of the 16 Data Boards.

2.0 DATA BOARD

2.1 FUNCTIONALITY

This board converts 16 fiber optic signals into TTL. They feed 16 differential drivers for remote transmission. There is also a 16 X 8 mux which is controlled by a VME FEC.

Each on board mux chip is configured as 8 16 X 1 muxes. Therefore the maximum number of cross connects is 8 per board. Since there are 16 boards there can be a maximum of 128 connections. To enable the FEC to monitor each board a 5-bit data latch has been implemented in the mux for each of the 8 16 X 1 muxes. They are VME addressable and can be read or written.

A four bit field selects 1 of the 16 inputs and the 5th bit determines the status of the 16 X 1 mux. Toggling this bit for the addressed latch either makes or breaks a cross connect for a selected input signal.

Each board is VME addressable. A 8 position DIP switch is used to establish 16 unique VME addresses.

Upon turning power on the VME SYSRESET* signal will clear all 128 5-bit latches. Each addressed board will have a separate reset* signal to clear the latches at the board level. Sixteen FEC issued resets will clear the entire 256 X 8 mux.

Each board will support a VME interrupt which will be initiated by the change of status of at least one of the fiber optic signals. The FEC will be able to determine which signals caused the interrupt by reading 2 status registers. This will clear the interrupt request until a subsequent change of a fiber optic signal occurs. A change is caused by either the loss or connection of a signal.

Each board will have an interrupt mask. Under FEC control it will determine which of the link statuses will be enabled to generate an interrupt.

Associated with each interrupt is a Vector and Routing Register. Both of which can be read and written by the FEC. The Routing Register under FEC control will determine which of the 7 interrupt lines will be enabled when the Data Board initiates an interrupt. Enabling interrupt 0 disables all interrupts. When an interrupt is implemented the contents of the FEC controlled Vector Register is transmitted to the FEC so it can identify the initiator.

2.2 HARDWARE ARCHITECTURE

2.2.1 SYSTEM BUS

The Data Board is a slave with 8 addressable 5-bit latches. This board will respond to address modifier codes for supervisory and non-privileged short (A16) access. This board will occupy a 256-byte contiguous block of address space on the VME backplane. The base address is configurable by a DIP switch and can be located on any 256-byte boundary within a 64K-byte address space. An 8 bit data bus shall be implemented to return all data structures and this board supports D08(O) Data Bus Transfer cycles. Block Transfer (BLT) and Read-Modify-Write (RMW) bus cycles are not permitted. This slave will also decode the DS0*, DS1*, LWORD*, IACK8, and A01 control lines. VME handshake protocol lines such as DTACK*, WRITE*, and AS* will also be supported. Generation of a BERR* signal on the VME bus will not be implemented. This board has provision to either generate or respond to interrupts.

2.2.2 I/O INTERFACE

2.2.2.1 OUTPUTS

The output of the Data Board for the converted TTL signals will be via differential drivers. The J3/P3 connector will be wired to a backpanel bulkhead connector with a 64 wire ribbon cable.

A tri-stated driver will be used to drive the 8 signal outputs of the mux chip onto the J2/P2 backplane. The status bit from each of the 8 latched data registers will control the driver. The 17 slot backplane will be terminated at each end.

2.2.2.2 INPUTS

The fiber optic cables will be terminated through the front panel. A fiber status LED will be displayed through the front panel.

2.3 VME BUS MASTER COMMUNICATIONS PROTOCOL

There is a status ID prom.

The communications protocol is as follows:

16 BIT ADDRESS	FUNCTION	READ/WRITE	DATA BYTE
X Y 0 0H	EVEN BYTE ID PROM	READ	2E H
X Y 0 1H	ODD BYTE ID PROM	READ	
TO	64 ID PROM BYTES		
X Y 3 EH	EVEN BYTE ID PROM	READ	2E H
X Y 3 FH	ODD BYTE ID PROM	READ	
X Y 4 1H	SEL DATA FOR OUT 0 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 3H	SEL DATA FOR OUT 1 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 5H	SEL DATA FOR OUT 2 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 7H	SEL DATA FOR OUT 3 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 9H	SEL DATA FOR OUT 4 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 BH	SEL DATA FOR OUT 5 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 DH	SEL DATA FOR OUT 6 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 4 FH	SEL DATA FOR OUT 7 ON BD XY	BOTH	0 0 0 0 S S3 S2 S1 S0B
X Y 5 1H	RESET ALL CROSS CONNECTS ON BD XY	WRITE	DO NOT CARE

X Y 5 3H	VECTOR REGISTER ON BD XY	BOTH						
X Y 5 5H	ROUTING REGISTER ON BD XY	BOTH						
X Y 5 7H	READ FIBER REC STATUS(LO) ON BD X	READ	L7	L6	L5	L4	L3	L2 L1L0B
X Y 5 9H	READ FIBER REC STATUS(HI) ON BD XY	READ	L15		TO			L8B
X Y 5 BH	LO ORDER MASK BYTE ON BD XY	BOTH	M7		TO			M0B
X Y 5 DH	HI ORDER MASK BYTE ON BD XY	BOTH	M15		TO			M8B

S = 1: Make connection for addressed 16 X 1 mux
S = 0: Break connection for addressed 16 X 1 mux
S3 S2 S1 S0: Address of the input to the 16 X 1 mux on board XY
XYS3 S2 S1 S0: Address of selected input signal (1 to 256) on 16 addressable boards
XY41H to XY4FH: Address of selected output (0 to 7) on board XY
Lx = 1: Loss of optical signal for fiber receiver (0 to 15) on board XY
Lx = 0: No loss of optical signal for fiber receiver (0 to 15) on board XY
Mx = 1: Mask out associated link status interrupt
Mx = 0: Enable associated link status interrupt

VME addresses XY41H to XY4FH select a 5-bit register which defines the state of each 16 X 1 mux. Writing this field permits the selection of up to 8 signals to be remotely transmitted. Since any combination of eight signals is possible connections will be made and broken to accommodate change. To insure that the limit of 8 is not exceeded, a readback of the data field is supported. Since there are 128 16 X 1 muxes no more than 128 readbacks are needed.

The upper part of the address field selects each board. Addresses XY41H to XY4FH are used to select the mux outputs. Address XY51H is the board reset of the 8 16 X 1 muxes. It breaks all cross connects between the 16 inputs and the 8 outputs for that addressed board. Sixteen resets will clear the system of all cross connects. The VME RESET signal will perform the same function for power on.

Each board has 16 fiber optic receivers with each having a status bit. It indicates the loss or presence of the optical signal. Upon a single or multiple loss or reconnection a priority interrupt will be initiated. The interrupt request level is determined by the Routing Register at VME address XY55H. The VME interface chip will respond to the IACKIN* with an IACK* and by returning the contents of the Vector Register (address XY53H) on the data bus. This informs the FEC which board has initiated the interrupt. The FEC then does 2 status reads to VME addresses XY57H and XY59H. The 2 data bytes will return the link status of all 16 fiber optic receivers. This will clear the interrupt until a new change is detected.

Each board can enable or disable each of the 16 interrupt conditions through a 16 bit Mask register. Under control of the FEC the Mask register can be read or written at VME addresses XY5BH and XY5DH. Enabling interrupt 0 in the routing register turns all interrupts off for that board.

2.4 ELECTRICAL SPECIFICATION

Voltages −5 V @ 3.5A

Each mux output TTL driver:
1. Will be tri-stated and will drive a terminated J2/P2 backplane
2. Terminations will be VME standard(470 and 330 ohm to +5 VDC)
3. Terminations will be at slots 5 and 21
4. Provides a minimum amplitude of 3.0 VDC at the J2/P2 connector
5. Outputs will wire-Ored with 15 other drivers through the backplane
6. Minimum pulse width of 35 nanosecs.
7. Frequency 8-10 MHz

Each TTL output driver:
1. Will be differential and will drive a terminated 100 ohm load

2. Meets EIA standard RS-422-A

The VME interface:
1. Will conform to the VME bus specification
2. Will only utilize the J1/P1 backplane

Each fiber optic receiver:
1. Will accept fiber sizes 50/125, 62.5 125, 85/125, and 100/140 um
2. Will have an optical wavelength for rated sensitivity of 825 to 900 nm
3. Has a maximum optical input power(peak) @ 10 minus 9 BER of 100uW
4. Will support data rates of 1 to 50 Mbits/s
5. Will output TTL signals
6. Will output the status of the link

2.5 PHYSICAL SPECIFICATION

• This board will be a 9U. 160mm standard VME size B board. It will occupy a standard 4HP chassis space.

Front panel indicators will include 16 LEDs which will indicate CHX Valid and a 17th LED to indicate FEC board selection.

Front panel inputs will include 16 ST-type optic connectors for the 16 incoming serial signals.

3.0 OUTPUT BOARD

3.1 FUNCTIONALITY

This board has 8 tri-stated receivers which are connected to the 8 bussed outputs of the 16 Data Boards. The bus is part of the J2/P2 backplane. The signals will be terminated on the backplane. These receivers are inputs to 8 fiber optic drivers for remote transmission.

3.2 HARDWARE ARCHITECTURE

3.2.2 I/O INTERFACE

3.2.2.1 OUTPUTS

This board will tap into the J2/P2 bus as inputs to the 8 fiber optic drivers. It will output the fiber cable through the front panel.

3.2.2.2 INPUTS

Eight tri-stated receivers connected to the J2/P2 backplane.

3.4 ELECTRICAL SPECIFICATION

Voltages +5 V @ 1.5A

Each input TTL receiver:
1. Will accept inputs from a terminated J2/P2 backplane
2. Terminations will be VME standard(470 and 330 ohm to +5 VDC)

3. Will accept TTL signals
4. Will sink at least 8 milliamp of output current

Each fiber optic driver:
1. Will accept fiber sizes 50/125, 62.5/125, 85/125, and 100/140 um
2. Will have an optical wavelength for rated sensitivity of 850 to 900 nm
3. Has a minimum peak optical power of 25.1uW
4. Will support data rates of dc to 50 Mbits/s
5. Will accept TTL signals

3.5 PHYSICAL SPECIFICATION

This board will be a 9U, 160mm standard VME size B board. It will occupy a standard 4HP chassis space.

Front panel fiber optic outputs will include 8 ST-type optic connectors for the 8 outgoing serial signals.